IN THE SPECIFICATION

Please amend the specification as follows:

[0003] Discrete decoupling capacitors are typically mounted adjacent to the IC die and connected to the conductors that provide power to the die. For a processor die, the die may be mounted on a substrate (e.g., an IC package), and a number of discrete capacitors may be mounted on the substrate along the periphery of the die and/or underneath the die. These capacitors are coupled to the power supply connections at the die through lands formed on the substrate. The capacitors may be used to store energy for use by the die during periods of non-steady state or transient current demands, or to manage noise problems that occur in the die.

[0014] Integrated circuit 110 may be a high-speed processor, which may be employed in computers, servers or network systems or otherwise and may be other types of circuits. In one embodiment, the integrated circuit 110 may be a semiconductor die or may be representative of one or more IC chips or a combination of different types of circuits including high-performance dies or chips, although not limited thereto. In the illustrated embodiment, an IC die 110 is shown which has bumps 115 (e.g., solder balls) mounted ~~115~~ on an upper surface of IC package 120. Alternatively, the integrated circuit 110 may be a surface mounted chip, in which input/output terminals thereof are connected to the IC package 120 using bond wires for connecting the chip to bonding pads at the upper surface of IC package 120. Although not shown herein, embedded capacitors may be incorporated within the integrated circuit 110 and/or the IC package 120, as deemed necessary.

[0018] In the illustrated embodiment, the array capacitor includes a number of first conductive layers 201, 203, 205, 207 and 209 interleaved with a number of second conductive layers 202, 204, 206, 208 and 210. Dielectric layers 211 through 220 separate adjacent conductive layers. The first conductive layers ~~201, 203, 205, 207 and 209~~ 202, 204, 206, 208 and 210 are configured to be coupled to a first node in a circuit. In an embodiment, the first node is a ground plane 230 provided in the IC package 120. The second conductive layers 201, 203, 205, 207 and 209 are configured to be coupled to a

second node in a circuit. In an embodiment, the second node is a power plane 235 provided in the IC package 120. The power plane 235 provides a positive potential to the second conductive layers. In an embodiment, the ground plane 230 and the power plane 235 are coupled to the integrated circuit 110 (e.g., semiconductor die) to provide electrical power and grounding to the circuits contained in the die.

[0025] It should be noted that because embodiments of the capacitors described herein are capable of being mounted ~~to~~ underneath an IC package ~~directly underneath the semiconductor die~~ and has openings to enables pins ~~located directly underneath the die~~ extending downward from the IC package to pass through, the package resistance can be reduced without sacrificing the package decoupling performance. In one embodiment, the capacitor described herein is used to satisfy high frequency noise and low frequency noise requirements of high-performance processors.